IN THE CLAIMS

Upon entry of the present amendment, the status of the claims will be as is shown below. The present listing of claims supersedes all previous versions and listings of claims in this application.

1-9 (Cancelled)

10 (Currently Amended) A digital signal processor, comprising:

an arithmetic logic unit configured to perform register-register arithmetic logic operations;

a plurality of registers configured to store data,

wherein the arithmetic logic unit is used to compare a first data with a second data and to output one of the first data and the second data based on a result of the comparison of the first data and the second data, in parallel with a comparison of a third data with a fourth data and an output of one of the third data and the fourth data based on a result of the comparison of the third data and the fourth data,

wherein the output one of the first data and the second data is provided as a ~~higher~~ first part of a processing data and the output one of the third data and the fourth data is provided as a ~~lower~~ second part of the processing data lower than the first part, and

wherein at least one of the plurality of registers stores the result of the comparison of the first data and the second data and the result of the comparison of the third data and the fourth data.

11. (Previously Presented) The digital signal processor according to claim 10, said

plurality of registers further comprising:

a first register and a second register,

wherein the first register stores the result of the comparison of the first data and the second data and the second register stores the result of the comparison of the third data and the fourth data.

12. (Previously Presented) The digital signal processor according to claim 11, wherein the first register and the second register are shift-registers.

13. (Previously Presented) The digital signal processor according to claim 10, wherein the arithmetic logic unit is configured to perform register-memory operations.

14. (Previously Presented) The digital signal processor according to claim 10, wherein the arithmetic logic unit is configured to perform a first addition, a second addition, a third addition and a fourth addition in parallel.

15. (Currently Amended) The digital signal processor according to claim 14, wherein the arithmetic logic unit is configured to add a first source processing data and a second source processing data in parallel with an addition of a third source processing data and a fourth source processing data, and each of the first, second, third and fourth source processing data is divided into a ~~higher~~ first part and a ~~lower~~ second part lower than the first part,

wherein the ~~higher~~ first part of the first source processing data and the ~~higher~~ first part of the second source processing data are added as the first addition,

wherein the ~~higher~~ first part of the third source processing data and the ~~higher~~ first part of the fourth source processing data are added as the second addition,

wherein the ~~lower~~ second part of the first source processing data and the ~~lower~~ second part of the second source processing data are added as the third addition, and

wherein the ~~lower~~ second part of the third source processing data and the ~~lower~~ second part of the fourth source processing data are added as the fourth addition.

16. (Previously Presented) The digital signal processor of claim 15,

wherein a result of the first addition is provided as the first data, a result of the second addition is provided as the second data, a result of the third addition is provided as the third data and a result of the fourth addition is provided as the fourth data.

17. (Currently Amended) A digital signal processor, comprising:

an arithmetic logic unit configured to perform register-register arithmetic logic operations;

a plurality of registers configured to store data,

wherein the arithmetic logic unit is used to compare a first data with a second data and to output one of the first data and the second data based on a result of the comparison of the first data and the second data, in a single cycle that also includes a comparison of a third data with a fourth data and an output of one of the third data and the fourth data

based on a result of the comparison of the third data and the fourth data,

wherein the output one of the first data and the second data is provided as a ~~higher~~ first part of a processing data and the output one of the third data and the fourth data is provided as a ~~lower~~ second part of the processing data lower than the first part, and

wherein at least one of the plurality of registers stores the result of the comparison of the first data and the second data and the result of the comparison of the third data and the fourth data.

18. (Previously Presented) The digital signal processor according to claim 17, said plurality of registers further comprising:

a first register and a second register,

wherein the first register stores the result of the comparison of the first data and the second data and the second register stores the result of the comparison of the third data and the fourth data.

19. (Previously Presented) The digital signal processor according to claim 18, wherein the first register and the second register are shift-registers.

20. (Previously Presented) The digital signal processor according to claim 17, wherein the arithmetic logic unit is configured to perform register-memory operations.

21. (Previously Presented) The digital signal processor according to claim 17,

wherein the arithmetic logic unit is configured to perform a first addition, a second addition, a third addition and a fourth addition in a single cycle.

22. (Currently Amended) The digital signal processor according to claim 21,

wherein the arithmetic logic unit is configured to add a first source processing data and a second source processing data in a single cycle with an addition of a third source processing data and a fourth source processing data, and each of the first, second, third and fourth source processing data is divided into a ~~higher~~ first part and a ~~lower~~ second part lower than the first part,

wherein the ~~higher~~ first part of the first source processing data and the ~~higher~~ first part of the second source processing data are added as the first addition,

wherein the ~~higher~~ first part of the third source processing data and the ~~higher~~ first part of the fourth source processing data are added as the second addition,

wherein the ~~lower~~ second part of the first source processing data and the ~~lower~~ second part of the second source processing data are added as the third addition, and

wherein the ~~lower~~ second part of the third source processing data and the ~~lower~~ second part of the fourth source processing data are added as the fourth addition.[[,]]

23. (Previously Presented) The digital signal processor according to claim 22, wherein a result of the first addition is provided as the first data, a result of the second addition is provided as the second data, a result of the third addition is provided as the third data and a result of the fourth addition is provided as the fourth data.